What is claimed is:

- 1 1. A current reference comprising:
- a current mirror circuit to force a first current to be substantially equal to a
- 3 second current;
- a control transistor coupled to the current mirror circuit to receive the first
- 5 current, the control transistor having first and second biasing terminals across which
- 6 a biasing voltage can be applied; and
- a variable resistor coupled between the first and second biasing terminals of
- 8 the control transistor and coupled to the current mirror to receive the second current.
- 1 2. The current reference of claim 1 wherein the variable resistor comprises a
- 2 plurality of resistive devices in parallel, each of the plurality of resistive devices
- 3 having a control input node to enable the resistive device.
- 1 3. The current reference of claim 1 further comprising a control loop circuit to
- 2 influence the variable resistor.
- 1 4. The current reference of claim 3 wherein the variable resistor comprises a
- 2 plurality of resistive devices in parallel, each of the plurality of resistive devices
- 3 having a control input node to enable the resistive device.
- 1 5. The current reference of claim 4 wherein the control loop circuit includes
- 2 output nodes, and wherein the control input node of each resistive device is coupled
- 3 to one of the output nodes of the control loop circuit.
- 1 6. The current reference of claim 4 wherein the control loop circuit comprises:
- a comparator to compare two voltages, the comparator having an output
- 3 node; and

- a state machine coupled to the output node of the comparator, the state
- 5 machine having output nodes coupled to the control input nodes of the plurality of
- 6 resistive devices.
- 1 7. The current reference of claim 1 wherein the control transistor comprises a
- 2 NFET, and the first and second biasing terminals are a gate source of the NFET.
- 1 8. The current reference of claim 7 further comprising a second NFET having a
- 2 drain terminal coupled to receive the second current from the current mirror, and
- 3 having a source terminal coupled to provide the second current to the variable
- 4 resistor.
- 1 9. The current reference of claim 1 further comprising a transistor coupled
- 2 drain-to-source between the current mirror and the variable resistor.
- 1 10. An integrated circuit comprising:
- a first current reference having a first current mirror with first and second
- 3 current paths, a first control transistor coupled in the first current path, and a first
- 4 variable resistor coupled in the second current path and across biasing terminals of
- 5 the first control transistor, the first current reference having an output node with
- 6 substantially constant current;
- a second current reference having a second current mirror with third and
- 8 fourth current paths, a second control transistor coupled in the third current path, and
- 9 a second variable resistor coupled in the fourth current path and across biasing
- 10 terminals of the second control transistor; and
- a control loop circuit having an input node coupled to an output node of the
- second current reference, and having an output node to influence the first and second
- 13 variable resistors.

- 1 11. The integrated circuit of claim 10 further comprising a voltage reference
- 2 having an output node coupled to a second input node of the control loop circuit.
- 1 12. The integrated circuit of claim 11 wherein the control loop circuit comprises
- 2 a comparator responsive to the second current reference and the voltage reference.
- 1 13. The integrated circuit of claim 12 wherein the control loop circuit further
- 2 comprises a state machine to influence the first and second variable resistors
- 3 responsive to the comparator.
- 1 14. The integrated circuit of claim 12 further comprising an output node coupled
- 2 to the output node of the second current reference to drive a resistor external to the
- 3 integrated circuit, and an input node coupled to the comparator to sample an external
- 4 voltage on the external resistor.
- 1 15. The integrated circuit of claim 10 wherein the first current mirror comprises
- 2 two PFET devices.
- 1 16. The integrated circuit of claim 10 wherein the first variable resistor includes a
- 2 first plurality of resistive devices in parallel, each of the first plurality of resistive
- 3 devices including an NFET and an n-well resistor.
- 1 17. The integrated circuit of claim 16 wherein the second variable resistor
- 2 includes a second plurality of resistive devices in parallel, each of the second
- 3 plurality of resistive devices including an NFET and an n-well resistor.
- 1 18. The integrated circuit of claim 17 wherein the control loop circuit is coupled
- 2 to a gate of the NFET in each of the second plurality of resistive devices.

- 1 19. The integrated circuit of claim 18 wherein the first and second control
- 2 transistors are NFET devices.
- 1 20. The integrated circuit of claim 10 wherein the first current reference further
- 2 comprises a transistor coupled in the second current path between the first current
- 3 mirror and the first variable resistor.
- 1 21. A current reference comprising:
- a control transistor having a gate terminal and a source terminal;
- a variable resistor coupled across the gate terminal and source terminal of the
- 4 control transistor, the variable resistor coupled to receive a generated current; and
- a control loop circuit responsive to a copy of the generated current, the
- 6 control loop circuit coupled to influence the generated current.
- 1 22. The current reference of claim 21 further comprising a current mirror coupled
- 2 to the control transistor and the variable resistor.
- 1 23. The current reference of claim 22 wherein the variable resistor comprises a
- 2 plurality of variable resistance devices coupled in parallel, each of the plurality of
- 3 variable resistance devices including an NFET responsive to the control loop circuit.
- 1 24. The current reference of claim 22 wherein the control loop circuit comprises a
- 2 comparator responsive to an output node of the current mirror.
- 1 25. The current reference of claim 24 wherein the control loop circuit comprises a
- 2 state machine responsive to the comparator to influence the variable resistor.
- 1 26. The current reference of claim 22 further comprising a transistor to support a
- 2 variable voltage between the current mirror and the variable resistor.

- 1 27. An integrated circuit comprising:
- a control transistor coupled in a first leg of a current reference circuit, the
- 3 control transistor having first and second biasing terminals;
- a variable resistor coupled in a second leg of the current reference circuit and
- 5 between the first and second biasing terminals of the control transistor; and
- a control loop circuit to modify a resistance value of the variable resistor, the
- 7 control loop comprising a variable impedance output driver.
- 1 28. The integrated circuit of claim 27 wherein the control loop circuit further
- 2 comprises:
- a comparator coupled to an output node of the variable impedance output
- 4 driver; and
- 5 a state machine responsive to the comparator.
- 1 29. The integrated circuit of claim 28 wherein the variable resistor comprises a
- 2 plurality of variable resistance devices coupled in parallel, each of the plurality of
- 3 variable resistance devices including an NFET responsive to the state machine.
- 1 30. The integrated circuit of claim 27 further comprising an output node
- 2 responsive to the variable impedance output driver to drive a resistor external to the
- 3 integrated circuit, and an input node to sample an external voltage on the external
- 4 resistor, and wherein the control loop circuit comprises:
- a voltage comparator to compare the external voltage and an internal voltage;
- 6 and
- a state machine responsive to the voltage comparator to influence the variable
- 8 resistor.